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(71) Applicant and
(72) Inventor: **OYHUS, Kim** [NO/NO]; Odvar Solbergs vei 90, N-0970 Oslo (NO).

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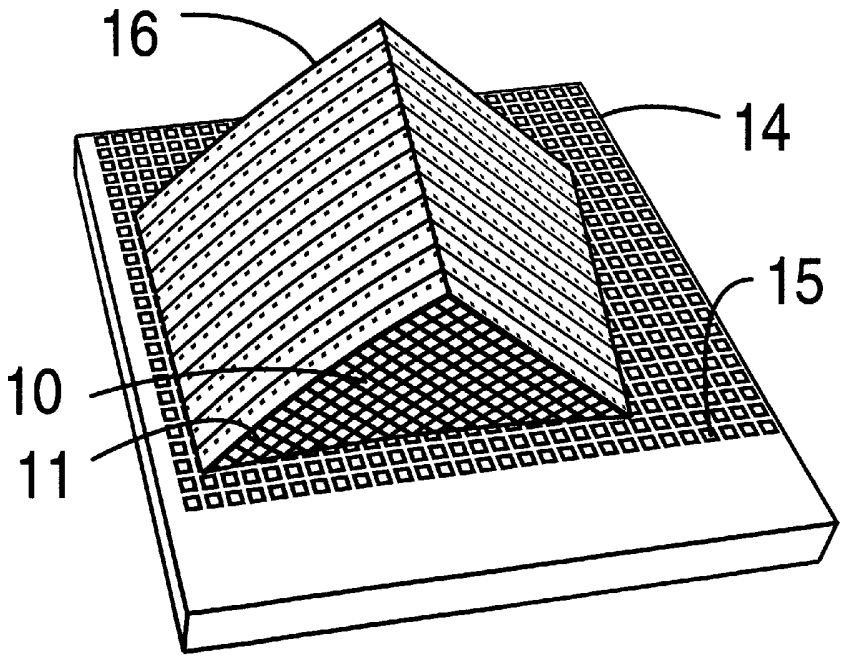
(54) **Title:** LAYERED CROSSBAR MEMORY CONNECTED TO INTEGRATED CIRCUIT



(57) **Abstract:** 3 dimensional electronic memory consisting of stacked thin layers (Fig 4) of crossbar memories, connected to surface of integrated circuit (14) (Fig 2) through crossbar connections (13) accessible by a diagonal cut (12) in the stack (Fig 1).

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layered memory

BACKGROUND OF THE INVENTION

The purpose of this invention, is to provide a cheap and simple way to efficiently fabricate 3-dimensional memory, possibly massive 3D memory.

Modern memories are typically 2 dimensional objects consisting of a few layers, such as integrated circuits built in a layering process, or stacked 2 sided magnetic plates, or layered DVDs with a transparent layer. One obvious way to produce larger memories is to increase the number of layers, but this introduces a lot of practical problems. In integrated circuits it increases process complexity and fault rate, due to the necessary precision and multiplication of an already complex process. For magnetic and optical plates there is the problem of multiplication of complicated, expensive, and large read/write heads. For holographic storage there is the problem of deformation of material.

An earlier example of ways of connecting layered memories is US-6,376,904 which is assigned to Rambus Inc, a company known for their memory technology. This patent regards stacking of interconnected integrated circuits, which can be memories. Disadvantages of this is the usually higher cost and complexity of integrated circuits, as compared to f.ex. simple lattices in thin film. Connecting integrated circuits together also require precision and accuracy in the form of precisely placed conductors, flow soldering, or film with contacts. None of these interconnections are microscopic.

It has been experimented with producing 3-dimensional memories by stacking layers of memories made from thin film electronics, such as in the Norwegian patent application NO-20001360, where the layers are connected together by stacking them very precisely in a

pyramid, so that end pads are aligned, and can be connected. That patent says that this makes vias, conductive holes in layers, unnecessary. As of the filing date of this patent, the company of that patent, Thin Film Electronics, is reported to have problems going beyond 8 layers.

A couple of major problems if one stacks many layers of thin films with memories and electronics, is that there are going to be large amounts of faulty electronics, and alignment problems in interconnecting the layers. If the complex electronics are removed, by using simpler cross-bar memories, then the problem of faulty electronics gets smaller. However, the problem of connecting millions to billions of crossbar contacts precisely, when they come from different layers, possibly with variation in thickness and crossbar distances, seems insurmountable.

BACKGROUND OF THE INVENTION-OBJECTS AND ADVANTAGES

Some objects and advantages of the example of the invention are:

(a) The crossbar memories can be simply stacked, with no interconnections. No strips like in the prior art patent.

(b) Great precision is not needed in fabrication of thin crossbar memories. The crossbars can be uneven, vary in thickness, have cuts and short circuits, and be warped and bent. The thin crossbar-memories can have variable thickness, and non-rectangular cross sections in the crossbars. All provided that the crossbar memories still can be stacked, and the errors are not overly excessive.

(c) Crossbar memories are simple devices. Much simpler than most integrated circuits. They can lack complex electronic logic. This

makes their production simpler, and thus cheaper.

(d) Connection of millions to billions of conductors from crossbar memories are simplified to the conductively fastening of one cut surface of stacked memories to an integrated circuit. This is mentioned in claims 1 and 4.

(e) All control circuitry and error correction circuitry are accessed through, or embedded into, an integrated circuit

(f) It is possible to make massive memories by using large, and/or numerous stacks of crossbar memories, connected to one or more integrated circuits. One can envision a liter of memory, laying like a big wedge on a whole wafer of integrated circuits. Storing 1 bit per crossbar crossing, and having 1 um distance between them, could give 100 000 GB of storage.

(g) The stacking of thin film crossbar memories, they are mentioned in claim 3, can be done industrially by rolling the film up and cutting it to the required wedges, or other shapes with the diagonal cut. The slight bend that this gives to the stack, is not a problem for alignment.

(h) Thermal expansion and physical stresses can be alleviated by having the stack bent and skewed, thus giving more material flexibility. This reduces the need of having materials with compatible thermal expansion coefficients.

(i) Price. This device should be cheap to manufacture. Cost should be comparable to one integrated circuit.

Further objects and advantages will become apparent from a consideration of the ensuing description and drawings.

SUMMARY

3 dimensional electronic memory consisting of stacked thin layers (Fig 4) with crossbar memories, where the crossbars are diagonally cut (12)(Fig 1) such that the crossbar conductors (13) are connected to the surface of an integrated circuit (13)(Fig 2).

DRAWINGS--FIGURES

Drawings are not to scale, as there is no preferred scale.

FIG 1 shows a perspective view of a diagonally cut stack of crossbar memories. The cut is visible below the front layer.

FIG 2 shows a perspective view of the cut crossbar memory, attached to an integrated circuit.

FIG 3 shows the intersection between the integrated circuit and the cut crossbars. The pads on the integrated circuit are represented as simple squares to make the figure visually understandable. The pattern of connections are quite disordered.

FIG 4 shows a layer of cut crossbar memory.

DRAWINGS--Reference Numerals

10 The front most layer of crossbar memory in the stack.

11 A crossing point of 2 different conducting bars in a memory.

12 The diagonal cut in the stack. The cut of all crossbars are visible.

13 A cut bar in the diagonal cut.

14 An integrated circuit.

15 A contact pad on the integrated circuit.

16 A side of the stack, not the diagonal cut. Only half the bars are visible.

DETAILED DESCRIPTION--FIG 2 -PREFERRED EMBODIMENT (s)

Crossbar memories are devices consisting of rows of electrically conducting bars in one layer, and columns in a different layer, such that the conductors of one layer cross near the conductors of the other layer. Between these layers there are many different solutions for storing data, such as organic fuses, light emitting and conduction changing polymers, PN semiconductor transitions, etc. The only demand of this invention is that the conductors are accessible through the crossbar, which can be uneven, have faults, and other angles between them than 90 degrees. An example of another angle would be the 60 degrees of hexagonal packing that would facilitate light activated crossbar memory by packing the lighted regions tighter.

A preferred embodiment of the invention, is in the form of a thin film made from special plastic, as mentioned in claim 3. This thin film have conducting bars printed on each side, so that they cross, thus making a crossbar. This thin film is sandwiched with insulating layers and rolled up in a roll. This roll is cut

approximately along the bars, into pieces. These pieces are again cut (12) diagonally relative to the crossbars, as in claim 4, making a wedge, like in Fig 1. The wedge is imprecisely connected to the integrated circuit (14) along the diagonal cut, like in Fig 2. This connection makes the conductive bars in the crossbar (13) connected with the pads on the integrated circuits (15) resulting in a disordered pattern of conductor connections as in Fig 3.

Alternative Embodiments

Hexagonal pads on the chip can also be an advantage. The size and distance between the pads are not specified, as they are dependent on the specific characteristics of the crossbar conductors. Nor are area of pads on the integrated circuit specified. One among other factors to be adjusted are probability of 2 or more bars connecting to 1 or more pads. As illustrated in Fig 4, an inexact double coupling need not result in a problem, just a "W" like crossing of conducting bars instead of an "X" like crossing.

The crossbars need not be as thin and flexible as in thin plastic film.

Having the crossbars cross several integrated circuits is an obvious possibility, as well as having several stacks of crossbars coupled to one integrated circuit.

It is possible to cut off the top of the wedge, so as to make the device flatter, to fit inside flatter packages. This means some loss of memory, especially if the stack is cut squarely.

Operation

The manner of using this memory device, consisting of layers of

crossbar memories, is to access the layers of memory through the integrated circuit. To access the memories, multiplexed connections to the conductors in the crossbars are necessary. To achieve these connections, the stack of memories is cut diagonally, so that all conductors in the stack are accessible on one plane side. This side is then connected to the surfaced of an integrated circuit to provide necessary multiplexing and possibility of necessary error correction and necessary adaption to misalignment of connectors to the chip.

To access a single memory element in a crossbar switch 11 (Fig 4), the integrated circuit activates the pads 15 (Fig 4) connected to the conducting bars which cross at the memory element 11 (Fig 4). This is the main principle of operation. Thus the integrated circuit can be viewed as a multiplexer to access the bars in the layered crossbar memories.

There are two overlapping strategies for ordered memory access of the device. A map of the connections of Fig 3 can be made by measuring the electric behavior between close pads to see if they are connected to crossing bars. This map can be used to order accessible memory units so they can appear to be contiguous. The other strategy is to avoid the map, and instead measure with each access, using hashing techniques to give the appearance of contiguousness. In either case, error correction methods has to be applied. This is known art in the designing of hard disks and error correction codes.

Conclusion, Ramification, and Scope

Accordingly, the reader will see that this invention can be used to make 3-dimensional memories efficiently and cheaply.

Although the description above contains specificities, these should not be construed as limiting the scope of the invention, but as merely providing illustrations of some of the presently preferred embodiments of this invention. Thus the scope of the invention should be determined by the appended claims and their legal equivalents, rather than by the examples given.

Claims: I claim:

1. A crossbar device, comprising:

(a) a stack, having a plurality of stacked layers with crossbars,

(1) where said stack of crossbars are cut diagonally relative to said crossbars in said stack,

(2) whereby said crossbars become conductively accessible on the surface of said cut of said stack, and

(b) an integrated circuit, at least one, having an array of conductive pads, said pads are connected to said surface of at least one of said stack, whereby said pads are disorderly and imperfectly connected to said crossbars.

2. Said crossbar device of claim 1 wherein said layers of crossbars are memory.

3. Said crossbar device of claim 2 wherein said layers of crossbar memories are thin film.

4. A method for production of memory, comprising:

(a) providing a stack, having a plurality of stacked layers with crossbar memories,
(b) cutting said stack of memories diagonally relative to said crossbars in said stack, whereby said crossbars become conductively accessible on the surface of the cut of said stack, and
(c) providing an integrated circuit, at least one, having

an array of conductive pads,

(d) connecting disorderly and imperfectly said pads to said surface of at least one of said stack.

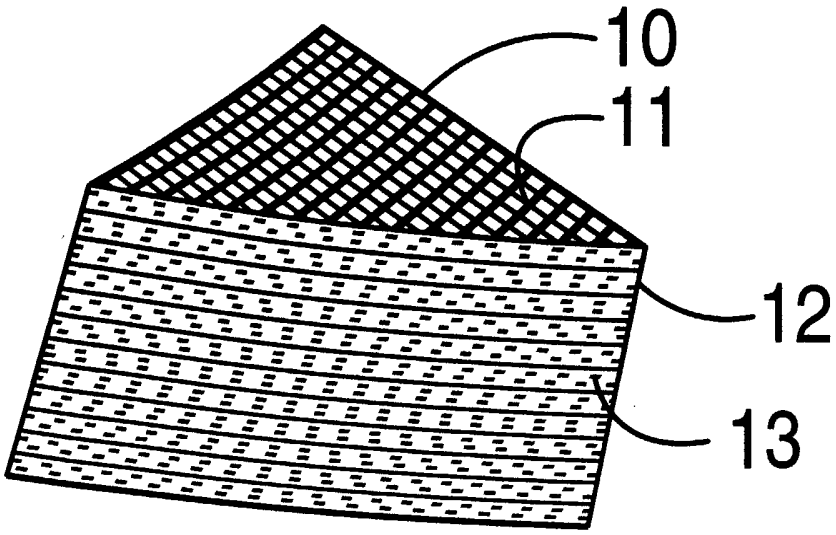

FIG.1

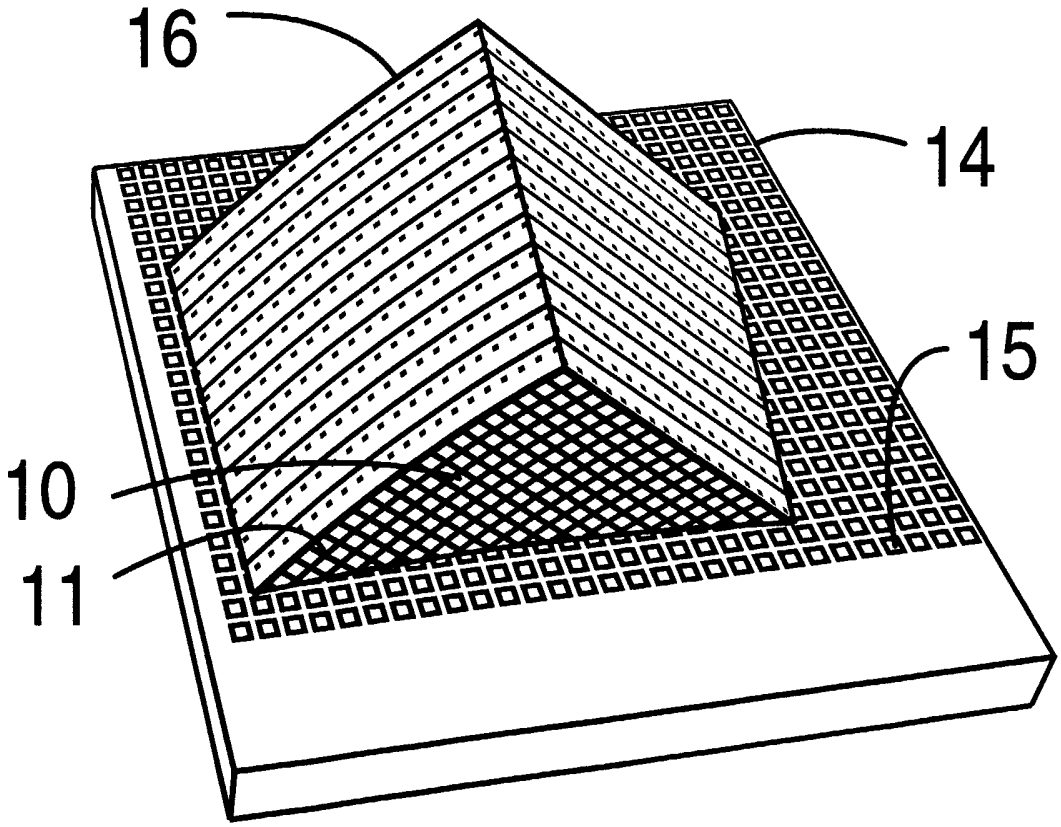

FIG.2

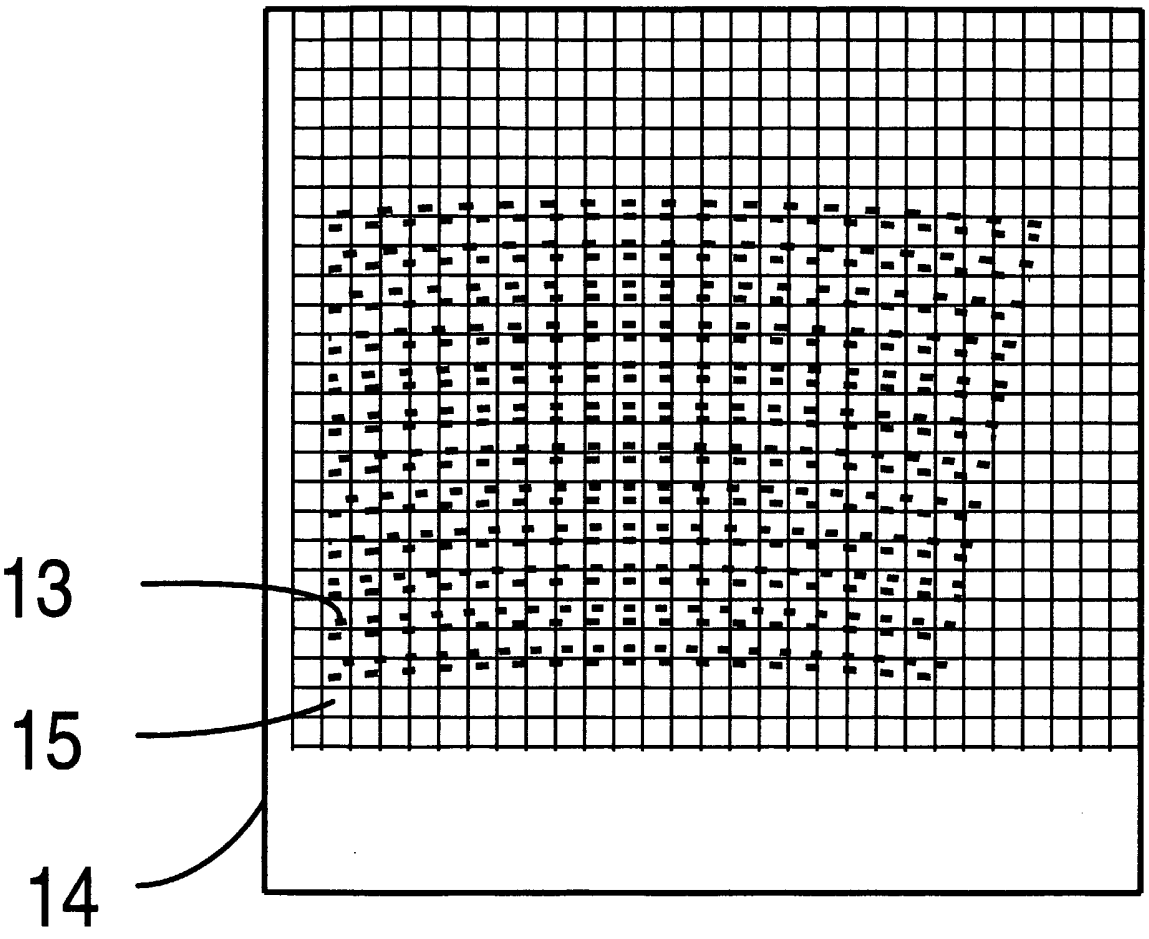

FIG.3

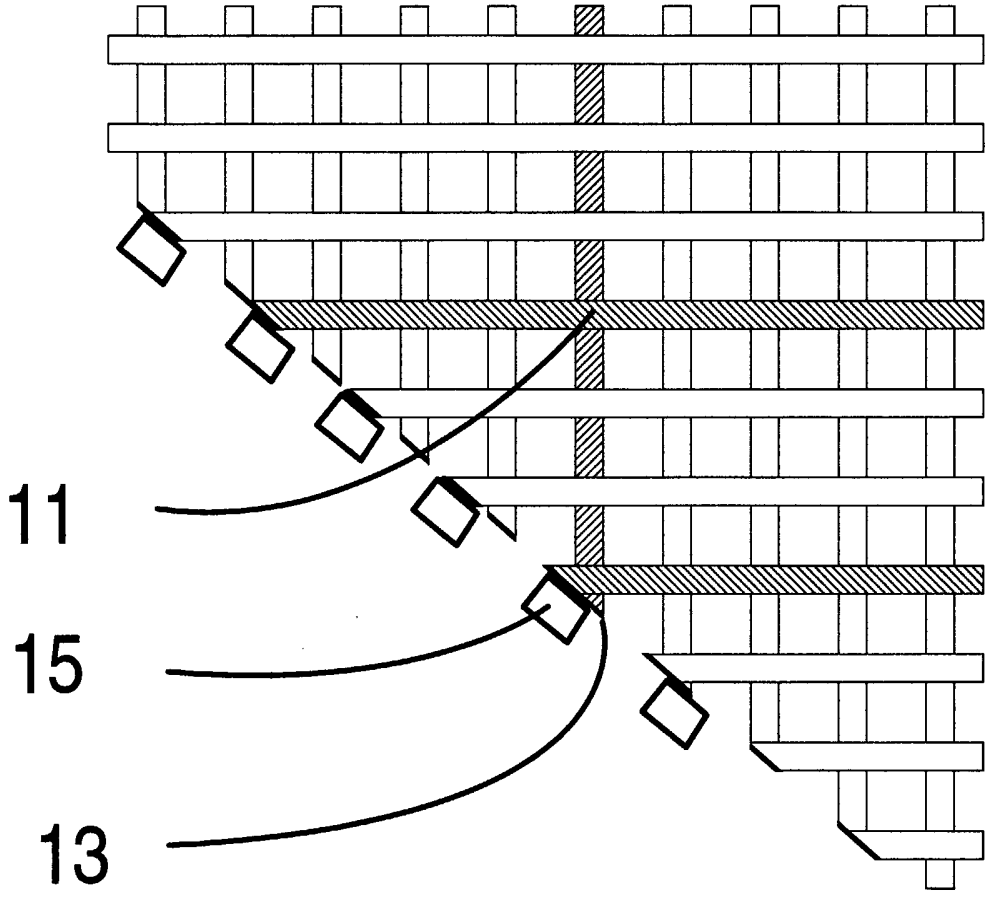

FIG.4

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/10 H01L27/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
11 May 2005	15/06/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Wirner, C

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 6 376 904 B1 (HABA BELGACEM ET AL) 23 April 2002 (2002-04-23) cited in the application figure 3a	1-4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
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